REMARKS

Claims 1-16 remain pending in the current Application. None of the claims have been amended, canceled, or added herein. The Examiner has rejected claims 1-16 under 35 U.S.C. 102(b) as being anticipated by US Patent No. 5,057,997 (hereinafter referred to as Chang). However, Applicant respectfully disagrees. Applicant submits that claims 1-16, as filed, are not taught or suggested by Chang.

Claim 1 requires providing a first storage device, which provides one or more hardware-generated interrupt signals, and a second storage device, which provides one or more software, generated signals. Claim 1 further requires logic circuitry coupled to both the first and second storage devices. While Chang discloses a hardware interrupt register, Chang makes no mention of a software interrupt register. The Examiner states that the second storage device is anticipated by instruction store 12 of FIG. 1; however, this is incorrect. Instruction store 12 of Chang stores software instructions, which may include instructions that cause software interrupts, but instruction store 12 does not receive and store software-generated interrupt signals, as claimed in claim 1. Furthermore, the Examiner states that logic circuitry of claim 1 is anticipated by interrupt circuits 18 of FIG.1 of Chang. However, interrupt circuits 18 is not coupled to receive hardware-generated and software-generated interrupt signals, as claimed in claim 1. Interrupt circuitry 18 of Chang compares the hardware interrupt register to an active contexts register (and not to a software interrupt register) to determine the highest found priority of interruption (e.g. see col. 6, line 30-40; see also col. 4, lines 45-67). This determination of the highest found priority is then used to determine whether to change the current context by comparing this highest found priority with the priority of the current context stored in register 32 (e.g. see col. 6, lines 40-53; see also col.5, lines 1-26). Therefore, there is no teaching or suggestion in Change of a storage device for receiving and storing software-generated interrupt signals in addition to a storage device for receiving and storing hardware-generated interrupt signals and logic circuitry coupled thereto. Therefore, for at least these reasons, claim 1 is not taught or suggested by Chang.

Claims 2-8 all depend directly or indirectly from claim 1 and are therefore allowable for at least those reasons mentioned above with reference to claim 1.

Claims 9 and 14 also require hardware interrupt storage, software interrupt storage, and logic circuitry coupled thereto, similar to claim 1. Therefore, the arguments provided above for claim 1 also apply to claims 9 and 14; therefore, claims 9 and 14 are not taught or suggested by Chang and are therefore allowable. Claims 10-13 and claims 15-16 all depend directly or indirectly from claims 9 or 14, are therefore allowable for at least those reasons mentioned above with reference to claim 1 which also apply to claims 9 and 14.

Conclusion

Although Applicant may disagree with statements made in reference to some of the dependent claims, Applicant is not discussing all these statements in the current Office Action, yet reserves the right to address them at a later time if necessary.

In view of the amendments and remarks set forth herein, the application is believed to be in condition for allowance and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is requested to telephone the undersigned at (512) 996-6839.

Respectfully submitted,

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